Form 1449 (Modified)	Atty Docket No.	Application No.:
	FULCP004X1	10/620,330
Information Disclosure Statement By Applicant	Applicant: Eaton et al. .	
	Filing Date	Group
(Use Several Sheets if Necessary)	July 14, 2003	Not yet assigned

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
HR	A	6,038,656	03.14.00	Martin et al.	712	211	
HR	B	5,752,070	05.12.98	Martin et al.	712	33	
HR	C	6,044,061	03.28.00	Aybay et al.	370	230	
HR	D	5,832,303	11.03.98	Murase et al.	710	36	

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
HR	E	Andrew Matthew Lines, Pipelined Asynchronous Circuits, June 1995, revised June 1998, pp. 1-37.
HR	F	Alain J. Martin, Compiling Communicating Processes into Delay-Insensitive VLSI Circuits, December 31, 1985, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-16.
HR	G	Alain J. Martin, Erratum: Synthesis of Asynchronous VLSI Circuits, March 22, 2000, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-143.
HR	H	U.V. Cummings, et al. An Asynchronous Pipelined Lattice Structure Filter, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-8.
HR	I	Alain J. Martin, et al. The Design of an Asynchronous MIPS R3000 Microprocessor, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-18.
HR	J	C.L. Seitz, System Timing, chapter 7, pp. 218-262.
HR	K	F.U. Rosemberger et al., Internally Clocked Delay-Insensitive Modules, IEEE Trans., Computers, vol. 37, no. 9, pp. 1005-1018, September 1998.
HR	L	U.S. Application 09/501,638, filed on February 10, 2000, entitled, Reshuffled Communications Processes in Pipelined Asynchronous Circuits.
HR	M	Lee et al., Crossbar-Based Gigabit Packet Switch with an Input-Polling Shared Bus Arbitration Mechanism, September 21, 1997, XVI World Telecom Congress Proceedings, Interactive Session 3 – Systems Technology & Engineering, pp. 435-441.
HR	N	Ghosh et al., Distributed Control Schemes for Fast Arbitration in Large Crossbar Networks, March 1994, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 2, No. 1, pp. 55-67.

Examiner Meler Kozrashek	Date Considered 02/19/04

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.